STIC Search Report
EIC 2800

STIC Database Tracking Number: 123527

TO: Monica Lewis **Location: JEF 5A30** **Art Unit : 2822** **Thursday, June 10, 2004** **Case Serial Number: 09/832867**	**From: Scott Hertzog** **Location: EIC 2800** **JEF4B68** **Phone: 272-2663** **Scott.hertzog@uspto.gov**

Search Notes

Examiner Lewis,

Attached are edited search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Hertzog

File 2:**INSPEC 1969-2004/**May W5
(c) 2004 Institution of Electrical Engineers
File 6:**NTIS 1964-2004/**Jun W1
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File 8:**Ei Compendex(R) 1970-2004/**May W5
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File 25:**Weldasearch 19662004/**Dec
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File 34:**SciSearch(R) Cited Ref Sci 1990-2004/**Jun W1
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File 65:**Inside Conferences 1993-2004/**Jun W1
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File 94:**JICST-EPlus 1985-2004/**May W3
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File 103:**Energy SciTec 1974-2004/**May B2
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(c) 2004 American Mathematical Society
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(c) 1999 Electric Power Research Inst.Inc
File 305:**Analytical Abstracts 1980-2004/**May W3
(c) 2004 Royal Soc Chemistry
File 315:**ChemEng & Biotec Abs 1970-2004/**May
(c) 2004 DECHEMA
File 987:**TULSA (Petroleum Abs) 1965-2004/**Jun W2
(c)2004 The University of Tulsa

Set	Items	Description
S1	26701	TFT OR (THIN(W)(FILM? ? OR LAYER? ?))(2N)TRANSIST?
S2	5612	IC=H01L-021? OR CC=B4260
S3	23096805	SECOND? OR ADDITIONAL? OR ADDED? OR FURTHER? OR 2ND OR TWO OR 2
S4	323174	GATE? ?
S5	831595	ELECTRODE?
S6	465	(S3(3N)S4)(3N)S5
S7	1079543	LUMINES? OR LIGHT(2N)(EMITT? OR EMISS?) OR LUMINES? OR EL OR ELD? ? OR PHOSPHOR? ? OR ELECTROLUMIN? OR PHOSPHORES? OR LED? ? OR ORGANOLUMIN? OR PHOSPHORES? OR OELD? ? OR ORGANIC(W)LED? ? OR OLED? ?
S8	0	S1:S2 AND S6 AND S7
S9	156078	(SI OR SILICON)(2N)(N OR O(N)N OR NITRIDE? ? OR OXYNITRIDE? ?)
S10	86289	SION OR SIN
S11	0	S8 AND S9:S10
S12	**1**	**S1:S2 AND S3 AND S4 AND S5 AND S7 AND S9:S10**
S13	33	S1:S2 AND S3 AND S4 AND S5 AND S7
S14	26	RD (unique items)
S15	9	S14 NOT PY>2000
S16	**9**	**S15 NOT S12**
S17	16097	CI=(SI BIN(S)N BIN) OR CI=(SI SS(S)O SS(S)N SS)(S)NE=3
S18	6	S17 AND S6
S19	6	S18 NOT S13
S20	6	RD (unique items)
S21	**5**	**S20 NOT PY>2000**
S22	848	CI=(TA BIN(S)N BIN)
S23	6565	CI=(TI BIN(S)N BIN)
S24	17597	S22 OR S23 OR CI=W EL
S25	11	S24 AND S6
S26	**1**	**S25 NOT PY>2000**
S27	275	S7 AND S24
S28	0	S27 AND S6
S29	479453	ELECTRODES OR (SECOND? OR ADDITIONAL? OR ADDED? OR FURTHER? OR 2ND OR TWO)(3N)ELECTROD?
S30	7	S27 AND S29
S31	6	S30 NOT PY>2000
S32	**6**	**S31 NOT S13**
S33	1603	S1 AND S7
S34	121394	N(N)(TYPE? ? OR CHANNEL? ?)
S35	63	S33 AND S34
S36	41578	(SECOND? OR ADDITIONAL? OR ADDED? OR FURTHER? OR 2ND OR TWO)(3N)(CONDUCT?(2N)(FILM? OR LAYER?) OR ELECTROD?)
S37	1	S35 AND S36
S38	28	S34 AND S36 AND S7
S39	25	S38 NOT S16 NOT S30 NOT S32 NOT PY>2000
S40	24	S39 NOT S37
S41	**16**	**RD (unique items)**

12/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

7728933 INSPEC Abstract Number: B2003-10-4260-006
Title: Light amplification in polymer field effect transistor structures
Author(s): Pauchard, M.; Swensen, J.; Moses, D.; Heeger, A.J.; Perzon, E.; Andersson, M.R.
Journal: Journal of Applied Physics vol.94, no.5 p.3543-8
Publication Date: 1 Sept. **2003** Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
Abstract: The amplified spontaneous emission (ASE) of optically pumped films of poly(**2**-(**2**',5'-bis(octyloxy)benzene)-1,4-phenylenevinylene (BOP-PPV) was studied in structures comprising a **gate electrode**, a thin film of **gate** insulator material (SiO/sub **2**/) and the polymer film as **luminescent** semiconducting layer (i.e. a field effect transistor without the source and drain **electrodes**). The influences of different **gate electrodes** on the threshold and the wavelength of the amplified emission were measured for variable thickness of the **gate** insulator. An exponential increase in ASE threshold (I/sub t/) with decreasing separation between **electrode** and polymer layer was observed. In structures with 200 nm SiO/sub **2**/ **gate** insulator, I/sub t/=300 kW/cm/sup **2**/ with an **n-Si gate electrode** and 200 kW/cm/sup **2**/ with Au **electrode** (100 nm thick). Compared to the same polymer film on pure SiO/sub **2**/ (I/sub t/=**2** kW/cm/sup **2**/), this increase results from waveguide losses in the nearby **gate electrode**. With an indium-tin-oxide (ITO) **gate electrode** (140 nm thick) on glass, again with a 200 nm SiO/sub **2**/ **gate** insulator, I/sub t/=30 kW/cm/sup **2**/. The ITO **electrode** acts as a **second** waveguide, and the light is distributed into **two** modes. The observed wavelength shift and the increasing I/sub t/ with decreasing SiO/sub **2**/ thickness result from this mode structure. When the thickness of the ITO **electrode** is less than 60 nm, the mode traveling mainly in the ITO is cutoff, and a single waveguide structure is formed with an associated reduction in I/sub t/. For an ITO thickness of 12 nm, I/sub t/=4 kW/cm/sup **2**/, only **two** times bigger than that observed in a pure BOP-PPV film on fused silica. (16 Refs)
Descriptors: insulated **gate** field effect transistors; **luminescent** devices; optical pumping; organic semiconductors; polymer films; superradiance
Identifiers: light amplification; polymer field effect transistor; amplified spontaneous emission; optical pumping; BOP-PPV film; poly(**2**-(**2**',5'-bis(octyloxy)benzene))-1,4-phenylenevinylene; **luminescent** semiconducting layer; **gate electrode**; SiO/sub **2**/ **gate** insulator; waveguide structure; ITO; Si; SiO/sub **2**/; Au; InSnO
Class Codes: **B4260** (Electroluminescent devices); B2560R (Insulated gate field effect transistors
Chemical Indexing:
Si int - Si el (Elements - 1)
SiO2 int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin (Elements - 2)
Au int - Au el (Elements - 1)

16/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:**INSPEC**

04344092 INSPEC Abstract Number: B9303-7260-043
Title: Improved driving method of a-Si **TFT** -LCD for HDTV LCD projection
Author(s): Katoh, K.; Adachi, M.; Matsumoto, T.; Tanaka, K.
Journal: Sharp Technical Journal no.54 p.35-8
Publication Date: **Nov. 1992** Country of Publication: Japan
CODEN: STEJD9 ISSN: 0285-0362
Abstract: A modification of the polarity inversion of source signals **led** to undesirable brightness differences in the pixels, and thereby a checkered pattern was revealed on the display under magnification. It was experimentally confirmed that this phenomenon occurred due to parasitic capacitance between a pixel **electrode** and a neighboring **gate** -line. An improved driving method where the first **gate**-signal of a pair has slight time lag behind the **second gate**-signal, can compensate for the capacitance. (8 Refs)
Subfile: B
Descriptors: amorphous semiconductors; high definition television; liquid crystal displays; optical projectors; silicon; **thin film transistors**
Identifiers: liquid crystal display; **TFT**-LCD; HDTV LCD projection; polarity inversion; parasitic capacitance; driving method; time lag; amorphous Si
Class Codes: B7260 (Display technology and systems); B4150D (Liquid crystal devices); B6430C (High definition television)
Chemical Indexing:
Si int - Si el (Elements - 1)

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16/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:**INSPEC**

04259323 INSPEC Abstract Number: B9211-4260-006
Title: Polychromatic **light emission** in a submicron MIS structure
Author(s): Kopytkin, B.A.; Kukin, M.A.
Journal: Mikroelektronika vol.21, no.1 p.52-4
Publication Date: Jan.-Feb. **1992** Country of Publication: Russia
CODEN: MKETA9 ISSN: 0544-1269
Abstract: The occurrence of white **light emission** in a submicron MIS transistor structure operating in conditions of hot channel-electron generation which was observed to remain after the **gate electrode** voltage is removed is described. (14 Refs)
Subfile: B
Descriptors: elemental semiconductors; insulated **gate** field effect transistors; **light emitting** devices; semiconductor-insulator boundaries; silicon; silicon compounds
Identifiers: white **light emission**; semiconductors; polychromatic **light emission**; submicron MIS structure; submicron MIS transistor structure; hot channel-electron generation; Si-SiO/sub **2**/

Class Codes: **B4260** (Electroluminescent devices); B2560R (Insulated gate field effect transistors); B2530F (Metal-insulator-semiconductor structures

Chemical Indexing:

Si-SiO2 int - SiO2 int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin - Si el (Elements - 1,2,2)

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16/9/4 (Item 4 from file: 2)

DIALOG(R)File 2:**INSPEC**

02710597 INSPEC Abstract Number: B86050169

Title: The addressing of light valves in a printer by high-voltage TFTs and resistors with a large sheet resistance

Author(s): Lueder, E.; Moersch, G.; Kallfass, T.; Koger, K.

Journal: Proceedings of the S.I.D vol.26, no.3 p.217-22

Publication Date: **1985** Country of Publication: USA

CODEN: SIDPAA ISSN: 0734-1768

Abstract: For the addressing of a PLZT light valve of a printer with pels spaced 250 mu m apart, a **TFT** for 400 V and an N-doped Ta resistor with 25 k Omega / Square Operator were developed. Reactive sputtering followed by anodization provides a high-yield fabrication of the Ta/sub **2**/O/sub 5/ **gate** oxide. The high ohmic Ta layer for the resistors is also sputtered. During sputtering the power and the N/sub **2** / pressure are continuously readjusted due to the resistance of the growing film. The fabrication steps for the **gate** oxide and the resistors are compatible with the production of the TFTs and the other components of the addressing circuit. The transparency of the light valve can be changed from less than 1% to about 95% by applying an input voltage step of 20 V to the **gate** of a switching transistor, resulting in a 250-V step at the PLZT cell **electrodes**. (8 Refs)

Subfile: B

Descriptors: **electroluminescent** displays; printers; sputtering; **thin film transistors**

Identifiers: PLZT; lead lanthanide zirconide titanide; reactive sputtering; flat panel displays; addressing; light valves; printer; high-voltage TFTs; large sheet resistance; N-doped Ta resistor; anodization ; high-yield fabrication; Ta/sub **2**/O/sub 5/ **gate** oxide; N/sub **2**/ pressure; transparency; switching transistor

Class Codes: B2220E (Thin film circuits); **B4260** (Electroluminescent devices); B7260 (Display technology and systems

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16/9/5 (Item 5 from file: 2)

DIALOG(R)File 2:**INSPEC**

00860123 INSPEC Abstract Number: B76005154, C76004986

Title: Thin film display switches

Author(s): Brody, T.P.; Yu, K.K.

Issued by: Westinghouse Res. Labs., Pittsburgh, PA, USA

Publication Date: 7 May **1975** Country of Publication: USA 43 pp.

Report Number: 75-9G9-PRNTM-R1 Contract Number: N00014-71-C-0269

Availability: NTIS, Springfield, VA 22161, USA
Abstract: A **thin film transistor** with a floating **second gate** , capable of nonvolatile storage of analogue data, was the subject of the investigation. **Further** development resulted in a closely controlled, reproducible fabrication process and a higher voltage capability. A square matrix of X-Y addressable memory transistors was designed, laid out and fabricated in a single vacuum deposition cycle. Mask and substrate registration techniques were also improved. The finished memory matrices were coated with an **electroluminescent phosphor** providing a common transparent front **electrode** and sealing with a cover-glass for complete 40*40 element storage displays. The displays were operable up to 140 V peak-to-peak.
Subfile: B C
Descriptors: analogue storage; **electroluminescence**; **luminescent** devices; semiconductor storage devices; **thin film transistors**
Identifiers: **thin film transistor**; nonvolatile storage; square matrix; addressable memory transistors; vacuum deposition; substrate registration; **electroluminescent phosphor**; sealing; analogue storage; mask registration
Class Codes: B2550G (Lithography); B2560S (Other field effect devices); **B4260** (Electroluminescent devices); C5330 (Analogue storage

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16/9/6 (Item 6 from file: 2)
DIALOG(R)File 2:**INSPEC**

00049944 INSPEC Abstract Number: B69015311
Title: Three terminal injection **luminescence** device
Author(s): Blicher, A.; Kupsky, G.A.
Journal: RCA Technical Notes no.21 p.TN755-2 pp.
Publication Date: April **1968** Country of Publication: USA
CODEN: RCTNAV
Abstract: A novel three-terminal injection **luminescence** device comprises a disc-like structure having a substrate layer of N-type GaAsP. A ring-type layer of P-type GaAsP is formed on the upper surface of the substrate layer, adjacent the periphery thereof, as by diffusion, epitaxy, or alloying methods. An insulating layer, such as of SiO/sub 2/ or Sn/sub 3/N/sub 4/, for example, is deposited on the remainder of the upper surface of the substrate layer. Metalized **electrode** layers and are formed on the substrate layer and the laer respectively. A ring-type, metallized, **gate electrode** layer is deposited on the insulating layer adjacent the periphery thereof. A transparent metalized **gate** layer, such as of Au, SnO, or SnCl/sub 2/, is deposited on the remainder of the insulating layer.
Subfile: B
Descriptors: **light emitting** devices
Class Codes: **B4260** (Electroluminescent devices

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16/9/7 (Item 1 from file: 8)
DIALOG(R)File 8:**Ei Compendex**(R)

01796008 E.I. Monthly No: EI8509076763 E.I. Yearly No: EI85031779
Title: SELF-ALIGNED AMORPHOUS-SILICON **TFT** FOR LCD PANELS.
Author: Kawai, Satoru; Nasu, Yasuhiro; Yanagisawa, Shintarou
Corporate Source: Fujitsu Lab, Display Devices Lab, Atsugi, Jpn
Source: Fujitsu Scientific and Technical Journal v 21 n 2 Summer 1985 p 204-210
Publication Year: **1985**
CODEN: FUSTA4 ISSN: 0016-2523
Abstract: A self-aligned hydrogenated amorphous-silicon **thin-film transistor** (a-Si:H **TFT**) used for liquid crystal display (LCD) panels has been developed. In the fabrication process, successive film deposition of the **gate** insulator, active layer, and passivation layer is utilized in order to obtain stable performance. The process also uses low-temperature deposition of **phosphor**-doped a-Si:H and evaporated Ti/Al for the source and drain **electrodes**. The multiplexing capability of the LCD panels addressed by the TFTs was found to exceed 1,000 lines at video frequencies. Using these TFTs, a prototype LCD panel with 33 X 33 pixels and **2**. 9 lines/mm was built and successfully operated. (Edited author abstract) 10 refs.
Descriptors: *DISPLAY DEVICES--*Liquid Crystal; TRANSISTORS; SEMICONDUCTING SILICON--Amorphous
Identifiers: **THIN-FILM TRANSISTORS**
Classification Codes:
741 (Optics & Optical Devices); 714 (Electronic Components); 712 (Electronic & Thermionic Materials)
74 (OPTICAL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATIONS)

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16/9/8 (Item 1 from file: 94)
DIALOG(R)File 94:**JICST-EPlus**

03410892 JICST ACCESSION NUMBER: 97A0898015 FILE SEGMENT: JICST-E
Simultaneous Operation of Superconducting Field Effect Transistors.
NAKAMURA T (1); INADA H (1); IIYAMA M (1)
(1) Sumitomo Electric Ind., Ltd., Osaka, JPN
Jpn J Appl Phys Part 1, **1997**, VOL.36,NO.8, PAGE.5081-5085, FIG.10, TBL.1, REF.18
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
ABSTRACT: A new process was developed for preparing four superconducting field effect transistors (SuFET's) on a substrate. This process yielded the **gate** structure of YBa2Cu3O7-x/SrTiO3/YBa2Cu3O7-x (YBCO/STO/YBCO) and the contact structure of buried YBCO **electrodes**. The average Tc of the YBCO (100 nm)/STO (200 nm)/YBCO (5 nm) structures was 49.7 K and the I-V characteristics of **gate** STO were symmetric The temperature dependence of transconductance was larger compared with other SuFET's reported to date. **Furthermore**, we confirmed the operation of all the SuFET's on one substrate and **two** adjacent SuFET's connected in series. This device fabrication process also **led** to improved Tc values of ultrathin YBCO channels. (author abst.)
DESCRIPTORS: yttrium compound; copper compound; barium compound; oxide; high temperature superconductor; superconducting thin film; ultrathin film; superconducting device; junction FET; **thin film transistor**; strontium titanate; transition temperature; current-voltage characteristic; **gate** circuit; mutual conductance; electric resistance

BROADER DESCRIPTORS: rare earth element compound; transition metal compound ; 1B group element compound; alkaline earth metal compound; chalcogenide; oxygen group element compound; oxygen compound; superconductor; superconducting material; material; thin film; membrane and film; solid state device; FET; transistor; semiconductor device; strontium compound; titanate; oxoate; titanium compound; 4A group element compound; temperature; thermodynamic property; electrical characteristic; characteristic; circuit; resistance
CLASSIFICATION CODE(S): BM04043E

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16/9/9 (Item 2 from file: 94)
DIALOG(R)File 94:**JICST-EPlus**

03054174 JICST ACCESSION NUMBER: 97A0041644 FILE SEGMENT: JICST-E
Study on Field Emitter Array for High Definition Display.
SHIMAWAKI HIDETAKA (1)
(1) Res. Inst. of Electr. Commun., Tohoku University
Nissan Kagaku Shinko Zaidan Kenkyu Hokokusho(Research Projects in Review, Nissan Science Foundation), **1996**, VOL.19, PAGE.95-98, FIG.7, REF.2
JOURNAL NUMBER: X0726AAW ISSN NO: 0911-4572
ABSTRACT: The current control and the stabilization in field emission of **gated** field emitter arrays(FEAs) are the highest demand for applications to a flat panel display and other beam devices. By fabricating FEA monolithically with FET or **TFT**, the emission current will be controlled and stabilized by applying a few volts on the **gate** voltage of FET or **TFT**. We carried out preliminary experiments of the idea and showed that the controllability and the stability of the emission current from Si-FEA were significantly improved by an actively controlled FEA. For the application to a high definition display, **additionally**, the small cross talk in the emitted electron beam is required. We proposed a new FEA structure with the focusing **electrode** which surrounds an individual emitter or block of emitter arrays on the same plane on the **gate** of FEA. (author abst.)
DESCRIPTORS: negative **electrode**; flat panel display; cathodoluminescence; **thin film transistor**; FET; field emission
BROADER DESCRIPTORS: **electrode**; display device; equipment; **luminescence**; transistor; semiconductor device; solid state device; electron emission; particle emission; emission
CLASSIFICATION CODE(S): NC06030Q

21/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

6558505 INSPEC Abstract Number: B2000-05-0520F-087
Title: Single wafer CVD of silicon nitride for CMOS gate applications
Author(s): Pomarede, C.; Werkhoven, C.; Weidmann, J.; Bergman, T.; Gschwandtner, A.; Houssa, M.
Conference Title: Ultrathin SiO/sub 2/ and High-K Materials for ULSI Gate Dielectrics. Symposium p.147-54
Editor(s): Huff, H.R.; Richter, C.A.; Green, M.L.; Lucovsky, G.; Hattori, T.
Publisher: Materials Research Society, Warrendale, PA, USA
Publication Date: **1999** Country of Publication: USA xvii+615 pp.
Conference Date: 5-8 April 1999 Conference Location: San Francisco,
Abstract: The MESC/CTMC compatible, Advance 2500 cluster tool made by ASM is evaluated for the manufacturing of CMOS gate stack structures based on CVD silicon nitride rather than thermally grown silicon oxide as the gate dielectric material, and polysilicon as the **gate electrode** material. With **two** different CVD chemistries excellent growth characteristics and thickness uniformity control of the silicon nitride is demonstrated. Electrical assessment reveals lower leakage current as compared to silicon oxide and minimal hysteresis in C-V curves, even for gate stacks that have an equivalent oxide thickness below 1.5 nm. The best properties are for silicon nitride films that also have a low H/sub 2/ content. (4 Refs)
Descriptors: chemical vapour deposition; CMOS integrated circuits; dielectric thin films; leakage currents; silicon compounds
Identifiers: single wafer CVD; CMOS gate applications; gate stack structures; growth characteristics; thickness uniformity; leakage current; C-V curves; H/sub 2/ content; Si/sub 3/N/sub 4/
Class Codes: B0520F (Chemical vapour deposition); B2810 (Dielectric materials and properties); B2570D (CMOS integrated circuits)
Chemical Indexing:
Si3N4 int - Si3 int - N4 int - Si int - N int - Si3N4 bin - Si3 bin - N4 bin - **Si bin - N bin** (Elements - 2)

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21/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:**INSPEC**

03787456 INSPEC Abstract Number: B91002073
Title: Amorphous silicon thin film transistor with a buried double-gate structure
Author(s): Kaneko, Y.; Tsutsui, K.; Matsumaru, H.; Yamamoto, H.; Tsukada, T.
Conference Title: International Electron Devices Meeting 1989. Technical Digest (Cat. No.89CH2637-7) p.337-40
Publisher: IEEE, New York, NY, USA
Publication Date: **1989** Country of Publication: USA 913 pp.
Abstract: An amorphous silicon thin-film transistor (a-Si TFT) with a novel structure is described. A **second gate electrode** is introduced into a gate insulator of silicon nitride in addition to the conventional staggered a-Si TFT gate electrode. The performance of this TFT

is characterized in terms of geometry and operating conditions. Equivalent electron mobility up to 1.8 cm/sup 2//(V-s) is achieved for optimized designs. It is also confirmed that the newly developed TFT preserves high reliability. Results of I-V measurements demonstrated that the on-current of a buried double-gate (BD) TFT reaches three times that of a conventional TFT. The V/sub t/ shift of the BD-TFT is about one-third that of the conventional TFT for the same gate electric field. The performance is suitable for large-area, high-resolution liquid-crystal displays. (8 Refs)

Subfile: B

Descriptors: amorphous semiconductors; carrier mobility; elemental semiconductors; silicon; thin film transistors

Identifiers: buried double-gate structure; amorphous silicon thin-film transistor; **second gate electrode**; gate insulator; electron mobility; optimized designs; high reliability; I-V measurements; on-current; gate electric field; high-resolution liquid-crystal displays; Si-SiN

Class Codes: B2560R (Insulated gate field effect transistors)

Chemical Indexing:

Si-SiN int - SiN int - Si int - N int - SiN bin - **Si bin** - **N bin** - Si el (Elements - 1,2,2)

26/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

6874413 INSPEC Abstract Number: B2001-04-2560R-079
Title: Characteristics of TaN gate MOSFET with ultrathin hafnium oxide (8 AA-12 AA)
Author(s): Byoung Hun Lee; Choi, R.; Kang, L.; Gopalan, S.; Nieh, R.; Onishi, K.; Jeon, Y.; Wen-Jie Qi; Kang, C.; Lee, J.C.
Author Affiliation: Microelectron. Res. Center, Texas Univ., Austin, TX, USA
Conference Title: International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) p.39-42
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: **2000** Country of Publication: USA 871 pp.
ISBN: 0 7803 6438 4 Material Identity Number: XX-2001-00191
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 10-13 Dec. 2000 Conference Location: San Francisco, CA, USA
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Experimental (X)
Abstract: MOSFET's with equivalent oxide thickness of 8-12 AA have been demonstrated by using high-K gate dielectric thin films (HfO/sub **2**/) and TaN **gate electrode** . Both self-aligned (higher thermal budget process) and non-self-aligned process (low thermal budget as in the replacement gate process) were used and compared. Excellent electrical characteristics (e.g. S~68 mV/dec) and reliability characteristics (e.g. high E/sub BD/, low charge trapping and SILC) were also obtained. (8 Refs)
Subfile: B
Descriptors: dielectric thin films; hafnium compounds; MOSFET; tantalum compounds
Identifiers: MOSFET; ultrathin hafnium oxide; equivalent oxide thickness; high-K gate dielectric thin film; TaN gate electrode; self-aligned processing; thermal budget; nonself-aligned processing; electrical characteristics; reliability; 8 to 12 A; TaN-HfO/sub 2/
Class Codes: B2560R (Insulated gate field effect transistors)
Chemical Indexing:
TaN-HfO2 int - HfO2 int - TaN int - Hf int - O2 int - Ta int - N int - O int - HfO2 bin - TaN bin - Hf bin - O2 bin - **Ta bin** - **N bin** - O bin (Elements - 2,2,4)
Numerical Indexing: size 8.0E-10 to 1.2E-09 m

32/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

6373418 INSPEC Abstract Number: A1999-22-8115L-010, B1999-11-0520J-013
Title: Electrochemical fabrication of **luminescent** CaWO/sub 4/ and CaWO/sub 4/:Pb films on W substrates with anodic potential pulses
Author(s): Kyoung-Wook Min; Sun-il Mho; In-Hyeong Yeo
Journal: Journal of the Electrochemical Society vol.146, no.8 p. 3128-33
Publisher: Electrochem. Soc,
Publication Date: **Aug. 1999** Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Abstract: **Luminescent** polycrystalline films of CaWO/sub 4/ and CaWO/sub 4/:Pb/sup 2+/ have been prepared on tungsten substrates by applying low anodic potential pulses at tungsten **electrodes** in alkaline solutions containing calcium ion or calcium and lead ions. Anodically grown CaWO/sub 4/ films show weak **luminescence** and broad X-ray diffraction peaks. The **luminescence** band of the film is shifted toward a longer wavelength (red shift) compared with that of the CaWO/sub 4/ powder prepared by a conventional solid-stale method. By postannealing the anodically grown CaWO/sub 4/ film at high temperatures, **luminescence** intensities are enhanced, and the **luminescence** band maximum has been blue shifted to 420 nm. CaWO/sub 4/ films doped with a trace amount of Pb/sup 2+/ ion, electrochemically prepared in alkaline solutions containing calcium and lead ions, show a decrease in the intensity of **luminescence** maybe because of hydroxides or of hydrated water. By postannealing, the intensity of **luminescence** is enhanced dramatically, and the **luminescence** band maximum is red shifted to 444 nm in comparison to that of undoped CaWO/sub 4/ films. (11 Refs)
Subfile: A B
Descriptors: annealing; calcium compounds; electrodeposition; lead; optical films; photoluminescence; red shift; spectral line intensity; spectral line shift
Identifiers: electrochemical fabrication; **luminescent** CaWO/sub 4/; CaWO/sub 4/:Pb films; W substrates; anodic potential pulses; **luminescent** polycrystalline films; tungsten substrates; low anodic potential pulses; alkaline solutions; anodically grown CaWO/sub 4/ films; weak **luminescence**; broad X-ray diffraction peaks; red shift; post-annealing; **luminescence** intensities; blue shift; hydrated water; 420 to 440 nm; CaWO/sub 4/:Pb; W
Class Codes: A8115L (Deposition from liquid phases (melts and solutions)) ; A4280X (Optical coatings); A7865P (Optical properties of other inorganic semiconductors and insulators (thin films/low-dimensional structures)); A6855 (Thin film growth, structure, and epitaxy); A8245 (Electrochemistry and electrophoresis); A7855H (Photoluminescence in other inorganic materials); A8140G (Other heat and thermomechanical treatments); A8140T (Optical properties (related to treatment conditions)); B0520J (Deposition from liquid phases); B4110 (Optical materials); B4190F (Optical coatings and filters)
Chemical Indexing:
CaWO4:Pb ss - CaWO4 ss - WO4 ss - Ca ss - O4 ss - Pb ss - O ss - W ss - Pb el - Pb dop (Elements - 3,1,4)
W sur - **W el** (Elements - 1)
Numerical Indexing: wavelength 4.2E-07 to 4.4E-07 m

41/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

6837152 INSPEC Abstract Number: A2001-06-4285D-001, B2001-03-4270-009
Title: Massively parallel low-cost pick-and-place of optoelectronic devices by electrochemical fluidic processing
Author(s): Ozkan, M.; Kibar, O.; Ozkan, C.S.; Esner, S.C.
Journal: Optics Letters vol.25, no.17 p.1285-7
Publisher: Opt. Soc. America,
Publication Date: **1 Sept. 2000** Country of Publication: USA
CODEN: OPLEDP ISSN: 0146-9592
Abstract: We describe a novel electrochemical technique for the nonlithographic, fluidic pick-and-place assembly of optoelectonic indium tin oxide (ITO) and **n-type** silicon substrates as the **two electrode** materials and deionized water (R=18 M Omega) as the electrolytic medium between the **two electrodes**. 0.8-20- mu m-diameter negatively charged polystyrene beads, 50-100- mu m-diameter SiO/sub 2/ pucks, and 50- mu m **LED**'s were successfully integrated upon a patterned silicon substrate by electrical addressing. In addition, 0.8- mu m-diameter beads were integrated upon a homogeneous silicon substrate by optical addressing. This method can be applied to a massively parallel assembly (>1000*1000 arrays) of multiple types (of devices of a wide size range) with very fast (a few seconds) and accurate positioning. (6 Refs)
Subfile: A B
Descriptors: electro-optical devices; electrochemistry; electrodes; integrated optics; integrated optoelectronics; **light emitting** diodes; optical fabrication; optoelectronic devices; parallel architectures ; substrates
Identifiers: massively parallel low-cost pick-and-place of optoelectronic devices; electrochemical fluidic processing; nonlithographic fluidic pick-and-place assembly; optoelectonic indium tin oxide; ITO; **n-type** silicon substrates; electrode materials; deionized water; electrolytic medium; negatively charged polystyrene beads; patterned silicon substrate; electrical addressing; homogeneous silicon substrate; massively parallel assembly; accurate positioning; 0.8 to 20 mum; 50 mum; SiO/sub 2/; InSnO
Class Codes: A4285D (Optical fabrication, surface grinding); A8245 (Electrochemistry and electrophoresis); A4282 (Integrated optics); B4270 (Integrated optoelectronics); B4260D (Light emitting diodes); B4150 (Electro-optical devices); B4140 (Integrated optics)
Chemical Indexing:
SiO2 int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin (Elements - 2)
InSnO int - In int - Sn int - O int - InSnO ss - In ss - Sn ss - O ss (Elements - 3)
Numerical Indexing: size 8.0E-07 to 2.0E-05 m; size 5.0E-05 m

+=
41/9/5 (Item 2 from file: 8)
DIALOG(R)File 8:**Ei Compendex**(R)

00587265 E.I. Monthly No: EI7612084365 E.I. Yearly No: EI76067010
Title: ELECTRICAL AND OPTICAL PROPERTIES OF GaSe-SnO//2 HETEROJUNCTIONS.
Author: Tatsuyama, Chiei; Ichimura, Shoji
Corporate Source: Toyama Univ, Takaoka, Jpn
Source: Japanese Journal of Applied Physics v 15 n 5 May 1976 p 843-847
Publication Year: **1976**
CODEN: JJAPA5 ISSN: 0021-4922
Language: ENGLISH
Journal Announcement: 7612
Abstract: GaSe-SnO//2 heterojunction structures were prepared in order to make **light emitting** diodes using GaSe. SnO//2 has a wide band gap energy about 3. 5 eV, and it is an **n-type** semiconductor. SnO//2 layer on the c-plane of GaSe was formed by using the spray method. These diodes have **emitted light** at considerably lower voltage compared with the diodes having **two electrodes** in the same c-plane of GaSe. In this paper, C-V and I-V characteristics, E. L. and photovoltaic effects at room temperature are reported. The forward I-V characteristics showed an space-charge-limited-current (SCLC) characteristic, which may originate in the high resistivity region produced by the diffusion of Sn into GaSe. The energy band model of GaSe-SnO//2 heterojunction is discussed. 17 refs.
Descriptors: SEMICONDUCTING GALLIUM COMPOUNDS; SEMICONDUCTOR DIODES, **LIGHT EMITTING**--Junctions; **ELECTROLUMINESCENCE**; PHOTOVOLTAIC EFFECTS
Classification Codes:
712 (Electronic & Thermionic Materials); 714 (Electronic Components); 741 (Optics & Optical Devices); 701 (Electricity & Magnetism)
71 (ELECTRONICS & COMMUNICATIONS); 74 (OPTICAL TECHNOLOGY); 70 (ELECTRICAL ENGINEERING)

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41/9/8 (Item 1 from file: 103)
DIALOG(R)File 103:**Energy SciTec**

04197115 NEDO-97-960224; EDB-97-105819
Title: Solar cell
Original Title: Taiyo denchi
Author(s)/Editor(s): Yamagishi, N.; Ueda, T.
Patent No.: **JP 9-36398**
Patent Assignee(s): Oki Electric Industry Co. Ltd., Tokyo (Japan)
Patent Date Filed: 25 Jul 1995
International Classification: H01L31/04
Publication Date: 7 **Feb 1997**
(5 p)
Journal Announcement: EDB9717
Abstract: The invented solar cell consists of the first **conductive** type emitter **layer** and the **second conductive** type base **layer**. The band gap of the emitter layer is made larger than that of base layer. Furthermore, the type two hetero junction interface is made between the emitter layer and the base layer. As a result, the light absorption efficiency of the incident **light** from the **emitter** layer side can be increased. At the junction interface between the emitter layer and the base layer, the discontinuous quantity of conductive band and the discontinuous quantity of valency

band occur. When the light comes into the junction interface, the light carriers are generated to elevate the Fermi level of the base layer side, resulting in the bend of the band. Unlike the conventional homo-cell type solar cell, the invented solar cell suppresses the generation of reverse direction current. So that a higher open circuit voltage and a higher conversion efficiency can be achieved. 4 figs.

Major Descriptors: **N-TYPE** CONDUCTORS -- ENERGY LEVELS; ***N-TYPE** CONDUCTORS -- HETEROJUNCTIONS; ***N-TYPE** CONDUCTORS -- INTERFACES; *P-TYPE CONDUCTORS -- ENERGY LEVELS; *P-TYPE CONDUCTORS -- HETEROJUNCTIONS; *P-TYPE CONDUCTORS -- INTERFACES; *SOLAR CELLS -- EFFICIENCY; *SOLAR CELLS -- PHOTOVOLTAIC CONVERSION

Descriptors: GRADED BAND GAPS

Broader Terms: CONVERSION; DIRECT ENERGY CONVERSION; DIRECT ENERGY CONVERTERS; ENERGY CONVERSION; EQUIPMENT; MATERIALS; PHOTOELECTRIC CELLS; PHOTOVOLTAIC CELLS; SEMICONDUCTOR JUNCTIONS; SEMICONDUCTOR MATERIALS; SOLAR EQUIPMENT

Subject Categories: 140501* -- Solar Energy Conversion -- Photovoltaic Conversion

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     FILE 'ZCAPLUS' ENTERED AT 14:30:45 ON 10 JUN 2004
                E N-CHANNEL/CT
                E TFT/CT
                E THIN FILM TRANSISTOR/CT
                E E4+NT,RT/CT
                E LIGHT EMITTING DEVICES+NT,RT/CT
                E LIGHT EMITTING DEVICES+ALL/CT
                E E2+NT,RT/CT

     INDEX 'CAPLUS, LCA' ENTERED AT 14:35:24 ON 10 JUN 2004
L1              QUE  ELECTROLUMINESCENT DEVICES/CT OR LED OR L E D
L2              QUE  (LIGHT(A)(EMITT? OR EMISS?))(A)(DEVICE# OR DIODE#) OR LUMINES? OR
                     EL OR ELD# OR PHOSPHOR# OR ELECTROLUMIN? OR PHOSPHORES? OR
                     ORGANOLUMIN? OR PHOSPHORES? OR OELD# OR ORGANIC(W) LED# OR OLED#
L3              QUE  L1 OR L2
L4              QUE  SECOND? OR ADDITIONAL? OR ADDED? OR FURTHER? OR 2ND OR TWO
L5              QUE  L4(3N)(ELECTRODE OR LAYER OR FILM) OR 2(2A)(LAYER? OR FILM? OR
                     ELECTRODE?)
L6              QUE  L3 AND L5
L7              QUE  OVERLAP? OR OVER(A)(HANG? OR LAP?) OR OVERHANG?
L8              QUE  L6 AND L7

     FILE 'HCAPLUS' ENTERED AT 14:47:19 ON 10 JUN 2004
L9            104 S L6 AND L7
     FILE 'ZCAPLUS' ENTERED AT 14:53:34 ON 10 JUN 2004
                E LDD/CT

     INDEX 'CAPLUS, LCA' ENTERED AT 14:58:13 ON 10 JUN 2004
L10             QUE  N(W)(CHANNEL OR TYPE)
L11             QUE  L9 AND L10

     FILE 'HCAPLUS' ENTERED AT 14:59:19 ON 10 JUN 2004
L12             3 S L9 AND L10
L13             3 S L12 AND P/DT
L14             8 S L8 AND H01L021?/IC
L15             7 S L14 NOT L13
     FILE 'WPIX' ENTERED AT 15:27:40 ON 10 JUN 2004
L16           29 SEA ABB=ON  PLU=ON  L14 NOT L13

     FILE 'HCAPLUS, WPIX' ENTERED AT 15:33:25 ON 10 JUN 2004
L17           33 DUP REM L15 L16 (3 DUPLICATES REMOVED)
                    ANSWERS '1-7' FROM FILE HCAPLUS
                    ANSWERS '8-33' FROM FILE WPIX
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☐ **L15 ANSWER 1 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:107875 HCAPLUS Full Text

Title

Method of manufacturing a thin film transistor semiconductor device for use in electrooptical devices

Author/Inventor

Arao, Tatsuya; Suzawa, Hideomi; Ono, Koji; Takayama, Toru

Patent Assignee/Corporate Source

Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002016028	**A1**	**20020207**	**US 2001-873334**	***20010605***
US 6596571	**B2**	**20030722**		
TW 501282	B	20020901	TW 2001-90113401	20010601
JP 2002064107	A2	20020228	JP 2001-172038	20010607
US 2004018670	**A1**	**20040129**	**US 2003-622584**	***20030721***

Dates too recent

Abstract

The present invention relates to a semiconductor device having a circuit constituted of thin film transistors (TFTs) and a method of manufacturing the same. More specifically, the present invention relates to an electrooptical device typified by a liquid crystal display panel and electronic equipment that mounts such an electrooptical device as its component. Conventionally, when a TFT provided with an lightly-doped drain structure or a TFT provided with a gate-drain ***overlapped*** lightly-doped drain (GOLD) structure is to be formed, there is a problem in that the manufacturing process becomes complicated, which increases the number of steps. An electrode formed of a lamination of a 1st conductive ***layer*** and a ***2nd*** conductive ***layer*** , which have different widths from each other, is formed. After the 1st conductive layer is selectively etched to form a 1st conductive layer, a low concentration impurity region ***overlapping*** the 1st conductive layer and a low concentration impurity region not ***overlapping*** the 1st conductive layer care formed by doping an impurity element at a low concentration

Concept or Classification

76-3 (Electric Phenomena) Section cross-reference(s): 74

Controlled or Index Terms

Dielectric films
Doping
Electric contacts
Electric insulators
Electroluminescent devices
Electrooptical imaging devices
Lamination
Projection apparatus
Semiconductor device fabrication
Thin film transistors
Video cameras
(method of manufacturing a thin film transistor semiconductor device for use in electrooptical devices)

National Patent Classification

438149000

International Patent Classification

ICM ***H01L021-00***
ICS H01L029-04; H01L031-036; H01L031-0376; H01L031-20; ***H01L021-84***

☐ **L15 ANSWER 3 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2000:861120 HCAPLUS Full Text

Title

Semiconductor devices having circuits formed by thin-film transistors and manufacturing method thereof

Author/Inventor

Yamazaki, Shunpei; Suzawa, Hideomi; Yamagata, Hirokazu

Patent Assignee/Corporate Source

Sel Semiconductor Energy Laboratory Co., Ltd., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
(1) EP 1058310	A2	20001206	EP 2000-111706	20000531
US 6583471	**B1**	**20030624**	**US 2000-583678**	***20000531***
JP 2001053287	A2	20010223	JP 2000-165617	20000602
US 2003201496	A1	20031030	US 2003-413736	20030415

Abstract

A semiconductor device comprises a first wiring on an insulating surface, a first interlayer insulating film covering the first wiring, and ***second*** interlayer insulating ***film*** in contact with a part of the first interlayer insulating ***film*** , and a ***second*** wiring on the first and ***second*** interlayer insulating ***film*** , wherein the first and ***second*** interlayer insulating ***films*** are laminated together in a region where the first and second wirings ***overlap*** with each other. The semiconductor devices include electrooptical devices, semiconductor circuits, and electronic equipments, which are formed by thin-film transistors, pixel circuits and driving circuits for controlling pixel circuits.

Concept or Classification

76-3 (Electric Phenomena)

Controlled or Index Terms

Electrochromic imaging devices
Electroluminescent devices
Projection apparatus
Video cameras
(application of semiconductor devices having circuits formed by thin-film transistors and manufacturing method thereof)
Dielectric films
Electrooptical imaging devices
Interconnections (electric)
Lamination
Liquid crystal displays
Luminescence , electroluminescence
Semiconductor device fabrication
Thin film transistors
(semiconductor devices having circuits formed by thin-film transistors and manufacturing method thereof)

International Patent Classification

ICM H01L027-12
ICS ***H01L021-84***

☐ **L15 ANSWER 4 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2000:335162 HCAPLUS Full Text

Title

Semiconductor device and method of manufacturing the same

Author/Inventor

Yamazaki, Shunpei; Adachi, Hiroki

Patent Assignee/Corporate Source

Semiconductor Energy Laboratory Co., Ltd., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
(1) EP 1001467	A2	20000517	EP 1999-122343	19991109
US 6617644	**B1**	**20030909**	**US 1999-432662**	**19991103**
JP 2000216396	A2	20000804	JP 1999-317714	19991109
US 2004051142	A1	20040318	US 2003-640939	20030814

Abstract

The present invention relates to a semiconductor device including a circuit composed of thin film transistors having a novel GOLD (Gate- ***Overlapped*** LDD (Lightly Doped Drain)) structure. The thin film transistor comprises a 1st gate ***electrode*** and a ***2nd electrode*** being in contact with the 1st gate electrode and a gate insulating film. Further, the LDD is formed by using the 1st gate electrode as a mask, and source and drain regions are formed by using the ***2nd*** gate ***electrode*** as the mask. Then, the LDD ***overlapping*** with the ***2nd*** gate ***electrode*** is formed. This structure provides the thin film transistor with high reliability.

Concept or Classification

74-13 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes) Section cross-reference(s): 76

Supplementary Terms

semiconductor device manuf thin film transistor ***electroluminescent*** display; liq crystal display gate ***overlapped*** lightly doped drain

Controlled or Index Terms

MOS transistors
(complementary; thin film transistor having novel gate-***overlapped*** LDD (lightly doped drain) structure for ***electroluminescent*** display and liquid crystal display)
Electroluminescent devices
Liquid crystal displays
Thin film transistors
(thin film transistor having novel gate-***overlapped*** LDD (lightly doped drain) structure for ***electroluminescent*** display and liquid crystal display)
7429-90-5, Aluminum, processes 7439-98-7, Molybdenum, processes
7440-25-7, Tantalum, processes 7440-32-6, Titanium, processes
7440-33-7, Tungsten, processes 7440-50-8, Copper, processes 11099-22-2
11106-92-6 12635-39-1 39306-00-8
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in conductive layer of thin film transistor having novel gate-***overlapped*** LDD (lightly doped drain) structure for ***electroluminescent*** display and liquid crystal display)

International Patent Classification

ICM H01L027-12
ICS ***H01L021-84***

☐ **L15 ANSWER 5 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1997:389112 HCAPLUS Full Text

Title

Semiconductor contact layer structure

Author/Inventor

Leadbeater, Mark Levence; Patel, Nalin Kumar; Burroughes, Jeremy Henley; North, Angus

Patent Assignee/Corporate Source

Toshiba Cambridge Research Centre Limited, UK

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
GB 2305003	A1	19970326	GB 1996-17283	19960816
GB 2305003	B2	19971008		
JP 09167876	A2	19970624	JP 1996-222796	19960823

Abstract

The semiconductor contact layer structure can be applied to a wide range of semiconductor devices. The layer configuration allows easy contact to be made to the layers and provides a method of isolating the active area of the device. A 1st contact layer is formed on a substrate and patterned to form a conducting substantially elongated section. A plurality of semiconductor layers are formed on top of the substrate and the 1st contact layer. The 1st contact layer can be seen through the plurality of semiconductor layers as a contact layer indent. A ***2nd*** contact ***layer*** is then formed on top of the plurality of semiconductor layers. The ***2nd*** contact ***layer*** is then patterned into a substantially elongated section which is oriented nonparallel to the 1st contact layer indent. The conduction region of the plurality of semiconductor layers is confined in the region by the ***overlap*** of the 1st and ***2nd*** contact ***layers***. The contact layers may form a Schottky gate, and the semiconductor device may be a resonant tunneling diode, a ***LED*** , or a laser.

Concept or Classification

76-2 (Electric Phenomena) Section cross-reference(s): 73

Controlled or Index Terms

Electroluminescent devices
Resonant tunneling diodes
Semiconductor devices
Semiconductor lasers
(contact layer structure for)

International Patent Classification

ICM ***H01L021-28***
ICS H01L029-88; H01S003-025

☐ **L15 ANSWER 6 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1982:226976 HCAPLUS Full Text

Title

Apparatus for gas-phase epitaxy of compound semiconductor

Patent Assignee/Corporate Source

Toshiba Corp., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 57027021	A2	19820213	JP 1980-102267	19800725

Abstract

An apparatus for epitaxially growing .gtoreq.***2*** compound-semiconductor ***layers*** with different compns. on a substrate from gas phase is described, which has a growth chamber in which the substrate is kept at a certain temperature, a number of gas-supply passages isolated from each other for supplying predetd. atms. of

reaction gases to the growth chamber, and a gas-supply-selection value between the growth chamber and passages. The selection value consists of 2 partition walls ***overlapping*** each other. The wall on the gas-supply-passage side has through holes for each gas-supply passages and the other has only 1 through hole. The desired reaction gases are introduced into the chamber through holes connected by relatively rotating the walls. Means of flowing an inert gas into the speces between the 2 walls are also provided to prevent unnecessary reaction gases from entering the reaction chamber. The apparatus is useful for the fabrication of semiconductor lasers and ***electroluminescent*** devices.

Concept or Classification

75-1 (Crystallography and Liquid Crystals) Section cross-reference(s): 73, 76

Supplementary Terms

gas phase epitaxy compd semiconductor; laser semiconductor gas phase epitaxy; ***electroluminescent*** device gas phase epitaxy

Controlled or Index Terms

Electroluminescent devices

(Group IIIA pnictides, gas-phase epitaxy for fabrication of, apparatus for)

International Patent Classification

H01L021-205 ; H01S003-18

☐ **L15 ANSWER 7 OF 7 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1980:560134 HCAPLUS Full Text

Title

Thin film transistor

Patent Assignee/Corporate Source

Westinghouse Electric Corp., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
GB 1565551	A	19800423	GB 1976-33948	19770106

Abstract

The manufacture is described of thin-film transistors with improved transconductance and high-voltage performance and reduced charge trapping, the transistors being particularly suitable for large-area flat ***electroluminescent*** display panels. The transistors are vapor deposited in successive steps on a glass substrate. An Al gate layer is deposited on the substrate and an Al oxide insulating layer is deposited over it, the gate extending beyond the insulating layer. A CdSe semiconductive layer is deposited on the insulating layer and overlays part of the gate. The CdSe layer contains sufficient In to stabilize the device. The CdSe layer forms a channel between the source and drain contacts which is .apprx.2-2.5 mils long for ***electroluminescent*** displays. Source and drain contacts ***overlap*** opposite sides of the channel and each comprises a 1000-Å-thick Cu layer on a 100-Å-thick In layer. A ***2nd*** Al oxide insulating ***layer*** is disposed over the source and drain contacts and a ***2nd*** Al gate ***electrode*** is positioned on the ***2nd*** insulating ***layer***.

Concept or Classification

76-13 (Electric Phenomena) Section cross-reference(s): 74

Supplementary Terms

thin film transistor ***electroluminescent*** display; ***luminescence*** electro flat panel display; cadmium selenide thin film transistor; indium doping cadmium selenide transistor

Controlled or Index Terms

Luminescent screens

(electro-, thin-film transistors for control and drive of, manufacture of)

Transistors
(thin-film, for ***electroluminescent*** flat-panel displays, manufacture of)
7440-74-6, uses and miscellaneous
RL: USES (Uses)
(thin-film transistors containing cadmium selenide doped with, for ***electroluminescent*** flat-panel displays)
1306-24-7, uses and miscellaneous
RL: USES (Uses)
(thin-film transistors containing indium-doped, for ***electroluminescent*** flat-panel displays, manufacture of)

International Patent Classification
H01L029-78; ***H01L021-363***

☐ **L17 ANSWER 8 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2004-224875 [21] WPIX Full Text

Title

Electroluminescent display device for electronic apparatus, has two electrodes overlapped with respective coloring layers, and film with laminates of portions overlapped with region, except light emitting portion of two pixels.

Author/Inventor

GOTO, Y; TANADA, Y; YAMAZAKI, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2004027055	**A1**	**20040212**	**(200421)***		**21**	**H01J001-62**
JP 2004094236	A	20040325	(200422)		17	G09F009-30

Application Details

US 2004027055 A1 US 2003-636869 20030807; JP 2004094236 A JP 2003-290913 20030808

Priority Application Information

JP 2002-233953	20020809

Abstract

US2004027055 A UPAB: 20040326

NOVELTY - The device has ***two*** coloring ***layers*** for different colors, and two pixels with respective pixel ***electrodes*** (157). The ***two electrodes*** are ***overlapped*** with the respective coloring layers. A film comprising a laminate of portions of the layers is ***overlapped*** with one of regions like a source signal line, gate signal line, and a thin film transistor, except a light emitting portion of the two pixels.

USE - Used for an electronic apparatus.

ADVANTAGE - The laminate of coloring layers is used to form the light-shielding portion, thus reducing a process for forming the light-shielding, which contributes to reduction of manufacturing cost and improvement of yield.

DESCRIPTION OF DRAWING(S) - The drawing shows a laminated structure of coloring layers.

Electrodes 153,154

Gate insulating film 155

Interlayer insulating film 156

Pixel electrodes 157

Banks 158

Dwg.1B/11

International Patent Classification

ICM G09F009-30; H01J001-62

ICS ***H01L021-336*** ; H01L029-786; H05B033-02; H05B033-14

☐ **L17 ANSWER 9 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2004-059389 [06] WPIX Full Text

Title

Semiconductor display device comprises pixel portion and semiconductor circuit that comprise thin film transistor comprising active layer, gate electrode, inorganic insulating films, and organic resin film.

Author/Inventor

HAYAKAWA, M; KATO, K; MURAKAMI, S; OSAME, M; YAMAZAKI, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003189210	**A1**	**20031009**	**(200406)***		**50**	**H01L029-04**
CN 1450665	A	20031022	(200406)			H01L031-12
JP 2003302917	A	20031024	(200406)		33	G09F009-30
KR 2003082385	A	20031022	(200415)			H01L029-786

Application Details

US 2003189210 A1 US 2003-400427 20030328; CN 1450665 A CN 2003-110353 20030409; JP 2003302917 A JP 2002-107216 20020409; KR 2003082385 A KR 2003-21881 20030408

Priority Application Information

JP 2002-107216	20020409

Abstract

US2003189210 A UPAB: 20040123

NOVELTY - A semiconductor display device comprises a pixel portion, and a semiconductor circuit comprising a capacitor. The pixel portion and the semiconductor circuit comprise a thin film transistor comprising an active layer, a gate electrode, a first inorganic insulating film, an organic resin ***film*** , and a ***second*** inorganic insulating ***film*** covering the organic resin film.

DETAILED DESCRIPTION - A semiconductor display device comprises a pixel portion, and a semiconductor circuit comprising a capacitor. The semiconductor circuit generates a signal for displaying an image on the pixel portion. The pixel portion and the semiconductor circuit comprise a thin film transistor. The thin film transistor has an active layer, a gate electrode adjacent to the active layer with a gate insulating film interposed in between, a first inorganic insulating film covering the thin film transistor, an organic resin film formed in contact with the first inorganic insulating ***film*** , and a ***second*** inorganic insulating ***film*** (7701) covering the organic resin film. The organic resin film has a first and a second opening part. The first and ***second*** inorganic insulating ***films*** are in contact with each other in the first and second opening parts. A contact hole is formed in the gate insulating film and the first and ***second*** inorganic insulating ***films*** in the first opening part such that the active layer is exposed. A wiring is formed on the ***second*** inorganic insulating ***film*** and is in contact with the active layer through the contact hole. The capacitor has a first electrode formed from the same conductive film as the gate ***electrode*** , a ***second electrode*** formed from the same conductive film as the wiring, and a part of the first and ***second*** inorganic insulating ***films*** that ***overlap*** the first ***electrode*** and the ***second electrode*** in the ***second*** opening part. A curvature radius of a surface of the organic resin film becomes longer continuously as the organic resin film separates from the first and second opening parts.

USE - As a semiconductor display device.

ADVANTAGE - The semiconductor display device uses an organic resin film as an interlayer insulating film, obtaining planarity of a surface of a surface of the interlayer insulating film while controlling film formation time, controlling time for heating treatment to remove moisture in the interlayer insulating film, and preventing moisture from being discharged to a film or an electrode adjacent to the interlayer insulating film.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor display device.

Cathode 7700

Second inorganic insulating ***film*** 7701
Electroluminescence layer 7702
Indium tin oxide 7703, 7704
Dwg.14B/29

International Patent Classification
ICM G09F009-30; H01L029-04; H01L029-786; H01L031-12
ICS G02F001-1333; G02F001-1368; G09G003-00; ***H01L021-00*** ; H01L027-00; H01L031-36; H05B033-14

☐ **L17 ANSWER 10 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number
2003-811323 [76] WPIX Full Text

Title
Manufacture of semiconductor device, e.g. dynamic random access memory, involves forming separated storage node contact plugs by burying conductive material in storage node contact holes in which insulating layer spacers are formed.

Author/Inventor
PARK, B J

Patent Assignee/Corporate Source
(PARK-I) PARK B

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003162353	A1	20030828	(200376)*		20	H01L021-8242 <--

Application Details
US 2003162353 A1 Div ex US 2002-107161 20020328, US 2003-334783 20030102

Priority Application Information

KR 2002-10205	20020226

Abstract
US2003162353 A UPAB: 20031125
NOVELTY - A semiconductor device is formed by forming separated storage node contact plugs by burying a conductive material in the storage node contact holes in which insulating layer spacers are formed.

DETAILED DESCRIPTION - Fabrication of semiconductor device comprises forming bit lines (125) on a semiconductor substrate on which cell pads (115a, 115b) are formed. The cell pads are separated from each other by an insulating layer. A bit line protection layer is formed on a surface of the substrate having the bit lines formed. The bit line protection layer has a thickness so that the bit lines are not buried. A first interlayer dielectric (ILD) film is formed on the bit line protection layer. It has a flat top and a thickness which is equal to or greater than a height of the bit lines. A ***second*** ILD ***film*** is formed on the first ILD film. It has a wet etch rate smaller than a wet etch rate of the first ILD film. Storage node contact holes are formed having narrow width by dry etching the ***second*** and first ILD ***films*** between the bit lines. They expose the cell pads. The width of the storage node contact holes is increased by wet etching the ***second*** and first ILD ***films*** , so that a lower width of each of the storage node contact holes is increased relatively more than an upper width of each of the storage node contact holes in view of the wet etch rates of the ***two*** ILD ***films***. Insulating ***layer*** spaces are formed on internal walls of the storage node contact holes. Separated storage node contact plugs (180) are formed by burying a conductive material in the storage node contact holes in which the insulating layer spacers are formed.

USE - For the fabrication of semiconductor device (claimed), e.g. dynamic random access memory.

ADVANTAGE - The method reduces the occurrence of shorts between the storage node contact plugs and bitlines and sufficient contact area between the storage node contact plugs and cell pads is obtained.

DESCRIPTION OF DRAWING(S) - The figure is a layout diagram of a DRAM having a capacitor over bit-line structure of the invention.

Cell pads 115a, 115b

Bit lines 125

Storage node contact plugs 180 Dwg.1/4

International Patent Classification

ICM ***H01L021-8242***

☐ **L17 ANSWER 11 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2004-068974 [07] WPIX Full Text

Title

Manufacture of pixel-defining layer on organic light emitting device involves using non-photosensitive polyimide or polyimide precursor compositions.

Author/Inventor

CHANG, Y; LU, T

Patent Assignee/Corporate Source

(RITD-N) RITDISPLAY CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003157740	A1	20030821	(200407)*		7	H01L021-00 <--

Application Details

US 2003157740 A1 Div ex US 2001-791556 20010226, US 2003-391606 20030320

Priority Application Information

TW 2000-107925	20000426

Abstract

US2003157740 A UPAB: 20040128

NOVELTY - Pixel-defining layer is formed on organic ***light emitting device*** panel by coating a layer of non-photosensitive polyimide or polyimide precursor compositions on a substrate with first electrodes. The substrate is first prebaked and then is baked to crosslink or cure the patterned non-photosensitive polyimide or polyimide precursor compositions.

DETAILED DESCRIPTION - Formation of pixel-defining layer on organic ***light emitting device*** (***OLED***) panel involves forming first electrodes (20) in parallel stripes on a substrate (10). A layer of non-photosensitive polyimide or polyimide precursor compositions is coated on the substrate with the first electrodes. The substrate is first prebaked and a layer of photoresist compositions is coated on the layer of the non-photosensitive polyimide or polyimide precursor compositions. Exposing the substrate to masked radiation and developing the photoresist form patterns of photoresist. The layer of the non-photosensitive polyimide or polyimide precursor compositions is etched to form a patterned layer of the non-photosensitive polyimide or polyimide precursor compositions. The patterned layer of the photoresist layer is released or stripped. The substrate with the patterned non-photosensitive polyimide or polyimide precursor compositions is baked to crosslink or cure the patterned non-photosensitive polyimide or polyimide precursor compositions and to form the pixel-defining layer (60).

An INDEPENDENT CLAIM is also included for ***OLED*** panel comprising first electrodes on a substrate, a non-photosensitive polyimide pixel-defining layers, photoresist ramparts (50) located on the first electrodes or the pixel-defining

layer, organic ***electroluminescent*** media on exposed area between the ramparts, and ***second electrodes*** located on the organic ***electroluminescent*** media. Each rampart protrudes from the substrate and has an ***overhanging*** portion projecting in a direction parallel to the substrate. The photoresist ramparts are formed through coating photoresist compositions on the substrate, exposing the substrate to masked radiation, and developing the photoresist.

USE - The method is used for forming pixel-defining layer on ***OLED*** panel (claimed). The ***OLED*** panel is used for display of televisions, computers, printers, screens, vehicles, signal machines, communication devices, telephones, lights, electric books, microdisplays, fishing machines, personal digital assistants, game machines, game goggles and airplanes.

ADVANTAGE - The cured polyimides having better thermal, electrical, mechanical and photochemical stability release organic solvent, which deteriorate the sensitive organic ***electroluminescent*** media of the ***OLED*** panels, thus extending the ***OLED*** panel lifetime. The polyimide pixel-defining layer on the ***OLED*** panel separates the anodes and cathodes effectively from electrical shorts.

DESCRIPTION OF DRAWING(S) - The figure is a partially enlarged perspective view of the ***OLED*** panel. Substrate 10

First electrodes 20

Ramparts 50

Pixel-defining layer 60

Auxiliary electrodes 70

Dwg.1/2

International Patent Classification

ICM ***H01L021-00***

☐ **L17 ANSWER 13 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-635857 [60] WPIX Full Text

Title

Light emitting device comprises thin film transistor over insulating surface having semiconductor layer, gate insulation film, and gate electrode.

Author/Inventor

MURAKAMI, S; SAKAKURA, M; TAKAYAMA, T; YAMAZAKI, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003129790	A1	20030710	(200360)*		51	H01L021-00 <--
CN 1419297	A	20030521	(200360)			H01L027-15
JP 2004047410	A	20040212	(200413)		35	H05B033-04

Application Details

US 2003129790 A1 US 2002-290478 20021108; CN 1419297 A CN 2002-157581 20021108; JP 2004047410 A JP 2002-324434 20021107

Priority Application Information

JP 2002-143800	20020517
JP 2001-345354	20011109

Abstract

US2003129790 A UPAB: 20030919

NOVELTY - ***Light emitting device*** comprises a thin film transistor over an insulating surface having a semiconductor layer (103), a gate insulation film

(108), and a gate electrode (110).

DETAILED DESCRIPTION - A ***light emitting device*** comprises a thin film transistor over an insulating surface having a semiconductor layer (103), a gate insulation film, and a gate electrode; first inorganic insulation layer (102) under the semiconductor ***layer*** ; ***second*** inorganic insulation ***layer*** (114) over the gate electrode; first organic insulation ***layer*** (115) over the ***second*** inorganic insulation ***layer*** ; third inorganic insulation layer (116) over the first organic insulation layer; wiring layer (117-125) extending over the third inorganic insulation ***layer*** ; ***second*** organic insulation ***layer*** (128) ***overlapping*** within a end of the wiring ***layer*** , the ***second*** organic insulation ***layer*** having an inclined surface with varying curvatures; fourth inorganic insulation layer (129) formed over an upper surface and a side surface of the ***second*** insulation ***layer*** , where the fourth inorganic insulation layer has an opening over the wiring layer; cathode layer (126) formed over the wiring layer, where the cathode layer and the fourth inorganic insulation layer; light emitting layer comprising an organic material formed over the cathode layer and the fourth inorganic insulation layer; an anode layer (131) formed over the light emitting layer comprising an organic material; and a fifth inorganic insulation layer (132) formed over the anode layer. The light emitted from the light emitting material is visible through the fifth inorganic insulation layer and the anode. Each of the third inorganic insulation layer and the fourth inorganic insulation layer comprises a material from silicon nitride or aluminum nitride.

USE - Used as organic ***electroluminescent*** display.

ADVANTAGE - The device has improved reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the construction of the light emitting apparatus.

Inorganic insulation layers 102, 114, 116, 129, 132
Semiconductor layer 103
Gate insulation film 108
Gate electrode 110
Wiring layer 117-125
Cathode layer 126
Anode layer 131
Organic insulation layers 115, 128 Dwg.1/32

International Patent Classification

ICM ***H01L021-00*** ; H01L027-15; H05B033-04
ICS G09F009-30; H01L033-00; H01L051-20; H05B033-00; H05B033-10; H05B033-14

☐ **L17 ANSWER 14 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-661145 [62] WPIX Full Text

Title

Light emitting device , e.g. video camera, includes light emitting elements having first light emitting region with first organic compound layer and second light emitting region with overlapping emitting layers.

Author/Inventor

HAMATANI, T; TAKAYAMA, T; YAMAZAKI, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003122140	A1	20030703	(200362)*		26	H01L033-00
CN 1428869	A	20030709	(200363)			H01L027-15
JP 2003257657	A	20030912	(200369)		19	H05B033-12

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
KR 2003057377	A	20030704	(200377)			H05B033-10

Application Details

US 2003122140 A1 US 2002-317615 20021212; CN 1428869 A CN 2002-160516 20021227; JP 2003257657 A JP 2002-376385 20021226; KR 2003057377 A KR 2002-83936 20021226

Priority Application Information

JP 2001-401687	20011228

Abstract

US2003122140 A UPAB: 20030928

NOVELTY - A ***light emitting device*** comprises light emitting element(s) containing a first light emitting region having a first organic compound layer between a cathode and anode (20) and a second light emitting region adjacent to the first region. The second region comprises ***overlapping two*** emitting ***layers*** between the cathode and anode.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a method of manufacturing the ***light emitting device*** comprising forming the anode from a transparent conductive film and a buffer layer covering the anode using same chamber, and forming a protective film on the buffer layer using a different chamber; and

(b) a manufacturing apparatus comprising a loading chamber, a first conveyor chamber, an organic compound layer ***film*** formation chamber, a ***second*** conveyor chamber, a metallic layer film formation chamber, a transparent conductive film formation chamber, a protective film formation chamber, a third conveyor chamber, a dispenser chamber, sealing substrate loading chamber and a sealing chamber.

USE - Used as a ***light emitting device*** i.e. video camera, digital camera, goggle display, car navigation system, personal computer or a portable information terminal.

ADVANTAGE - The device achieves high definition and a high aperture ratio in full color flat panel display. It prevents turning the ***light emitting device*** into a mirrored surface without using a polarizing film and provides a low cost ***light emitting device***.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the device.

Insulating film 15, 16

Anode 20

Buffer layer 32

Protective film 33

Dwg.1C/10

International Patent Classification

ICM H01L027-15; H01L033-00; H05B033-10; H05B033-12

ICS ***H01L021-00*** ; H01L051-20; H05B033-00; H05B033-04; H05B033-14

☐ **L17 ANSWER 15 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-558461 [52] WPIX Full Text

Title

Manufacture of semiconductor device, e.g. active matrix liquid crystal display device, involves the formation of gate electrode using one-step or two-step dry etching process.

Author/Inventor

OKAMOTO, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB; (OKAM-I) OKAMOTO S

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003100151	A1	20030529	(200352)*		45	H01L021-00 <--
JP 2003209260	A	20030725	(200357)		33	H01L029-786

Application Details

US 2003100151 A1 US 2002-287588 20021105; JP 2003209260 A JP 2002-323901 20021107

Priority Application Information

JP 2001-342212	20011107

Abstract

US2003100151 A UPAB: 20030813

NOVELTY - Semiconductor device is made by using a one-step or two-step dry etching process for the formation of a gate electrode. The etching process is performed to such a degree that a gate insulating film is exposed and a ***second layer*** gate ***electrode film*** is shorter in size in a channel direction than a first layer gate electrode film by using an etching gas containing fluorine, chlorine and oxygen.

DETAILED DESCRIPTION - Manufacture of a semiconductor device involves:

(a) forming an island-like semiconductor film over an insulating substrate;

(b) forming a gate insulating film (109) comprising an oxide film on the semiconductor film;

(c) forming a first layer gate electrode film (108) comprising tantalum nitride or tantalum on the gate insulating film;

(d) forming a ***second layer*** gate ***electrode film*** (107) comprising tungsten, a compound containing tungsten as a main constituent or tungsten nitride on the first layer gate electrode film;

(e) forming a mask on the ***second layer*** gate ***electrode film*** ; and

(f) performing an etching process to a degree such that the gate insulating film is exposed and the ***second layer*** gate ***electrode film*** is shorter in size in a channel direction than the first layer gate electrode film by using an etching gas containing fluorine gas, chlorine gas and oxygen with a predetermined chamber pressure, inductively coupled plasma (ICP) power density, bias power density, and flow ratio of the fluorine, chlorine and oxygen.

USE - Used for the manufacture of a semiconductor device e.g. semiconductor devices including a thin film transistor with a gate- ***overlapped*** lightly doped drain structure, and semiconductor display devices including an active matrix liquid crystal display device and an organic ***electroluminescent*** display device.

ADVANTAGE - Improves throughput in the dry etching step, reduces process cost as a result of reduced etching gas consumption, and improves the yield of a semiconductor device by suppressing defects and problems in association with a simplified dry etching step.

DESCRIPTION OF DRAWING(S) - The figure is a substrate section showing a one-step etching process.

Second layer gate ***electrode film*** 107

First layer gate electrode film 108

Gate insulating film 109

Dwg.1B/21

International Patent Classification

ICM ***H01L021-00*** ; H01L029-786

ICS ***H01L021-28*** ; ***H01L021-3065*** ; ***H01L021-336*** ; H01L029-423; H01L029-49

☐ **L17 ANSWER 17 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-414662 [44] WPIX Full Text

Title

Semiconductor device used in reflective liquid crystal display device, has electrode connected to scanning line at exterior of overlapping portion of electrode and semiconductor film.

Author/Inventor

YAMAZAKI, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB; (YAMA-I) YAMAZAKI S

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002039813	A1	20020404	(200244)*		35	H01L021-00 <--
JP 2002198537	A	20020712	(200261)		20	H01L029-786
US 6509616	B2	20030121	(200309)			H01L029-04

Application Details

US 2002039813 A1 US 2001-961525 20010925; JP 2002198537 A JP 2001-304290 20010928; US 6509616 B2 US 2001-961525 20010925

Priority Application Information

JP 2000-298304	20000929

Abstract

US2002039813 A UPAB: 20030928

NOVELTY - An electrode (133) is formed ***overlapping*** with the semiconductor films (107,108) formed on respective insulating layers. The electrode is connected to a scanning line (102) provided at the exterior of the ***overlapping*** portion of electrode and semiconductor films (107,108).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor device manufacturing method.

USE - Semiconductor device used in reflective liquid crystal display device of projector, electronic diary, mobile computer, portable telephone, video camera, still camera, personal computer, television. Also used in ***EL*** display device.

ADVANTAGE - The device provides the display unit with a high numerical aperture, without increasing number of processes. The manufacturing cost is reduced, since the number of mask manufacturing processes involved are reduced. As pixel electrode ***overlaps*** with wirings, thus the area of pixel electrode is increased.

DESCRIPTION OF DRAWING(S) - The figure shows the plan view explaining pixel structure manufacturing process.

Scanning line 102

Semiconductor film 107,108

Second shape ***electrode*** 133 Dwg.3/24

International Patent Classification

ICM ***H01L021-00*** ; H01L029-04; H01L029-786

ICS G02F001-1368; G09F009-30

☐ **L17 ANSWER 19 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-204934 [26] WPIX Full Text

Title

Semiconductor device manufacture by forming impurity region in semiconductor layer by doping impurity element into the semiconductor layer self-aligningly

using as mask the upper layer of gate electrode formed in two layers.

Author/Inventor

ONO, K; SUZAWA, H; TAKAYAMA, T

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB; (ONOK-I) ONO K; (SUZA-I) SUZAWA H; (TAKA-I) TAKAYAMA T

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC	
US 2002006705	A1	20020117	(200226)*		34	H01L021-00	<--
JP 2002083805	A	20020322	(200236)		30	H01L021-3065	<--
KR 2002017919	A	20020307	(200261)			H01L021-30	<--
TW 480576	A	20020321	(200308)			H01L021-00	<--
SG 100696	A1	20031226	(200414)			H01L021-336	<--

Application Details

US 2002006705 A1 US 2001-852282 20010510; JP 2002083805 A JP 2001-141133 20010511; KR 2002017919 A KR 2001-26005 20010512; TW 480576 A TW 2001-110576 20010503; SG 100696 A1 SG 2001-2817 20010511

Priority Application Information

JP 2000-193614	20000627
JP 2000-140999	20000512

Abstract

US2002006705 A UPAB: 20020424

NOVELTY - Semiconductor device is made by forming an impurity region in a semiconductor layer by doping an impurity element into the semiconductor layer self-aligningly using as a mask the upper layer of a gate ***electrode*** formed in ***two layers***.

DETAILED DESCRIPTION - Manufacture of semiconductor device comprises forming a semiconductor layer, forming a gate insulating film over the semiconductor layer, forming a first conducting film over the gate insulating ***film*** , forming a ***second*** conducting ***film*** over the first conducting film, forming a gate electrode of a first shape by carrying out dry etching at least once on the ***second*** conducting ***film*** and the first conducting film, forming a first impurity region in the semiconductor layer, forming a gate ***electrode*** of a ***second*** shape by carrying out dry etching on the gate electrode of the first shape, forming a gate electrode of a third shape by carrying out dry etching selectively on the ***second*** conducting ***film*** of the gate ***electrode*** of the ***second*** shape, and forming a second impurity region in the semiconductor layer.

USE - Used for the manufacture of a semiconductor device useful in a part of a display, particularly liquid crystal displays, organic ***electroluminescent*** (***EL***) displays (a ***light emitting device*** or a ***light emitting diode***) and electronic equipment using such displays. The ***EL*** devices include triplet-based ***light emission devices*** and/or singlet-based ***light emission devices***.

ADVANTAGE - The process reduces the number of masks required and eliminates trouble associated with the formation of these masks so reducing manufacturing cost of the semiconductor device and the time required for its manufacture.

DESCRIPTION OF DRAWING(S) - The figure shows a section of a reflective liquid crystal display.

Dwg.8/12

International Patent Classification

ICM ***H01L021-00*** ; ***H01L021-30*** ; ***H01L021-3065*** ; ***H01L021-336***

ICS ***H01L021-28*** ; H01L029-76; H01L029-786; H01L031-113; H01L031-36

☐ **L17 ANSWER 20 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2001-212813 [22] WPIX Full Text

Title

Semiconductor device, e.g. electroluminescent display device, comprises three wirings, three insulating films, semiconductor film, and gate electrode.

Author/Inventor

ISOBE, A; SHIBATA, H

Patent Assignee/Corporate Source

(SEME) SEL SEMICONDUCTOR ENERGY LAB; (SEME) SEMICONDUCTOR ENERGY LAB

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 1081676	A1	20010307	(200122)*	EN	38	G09G003-36
JP 2001144301	A	20010525	(200136)		19	H01L029-786
CN 1286493	A	20010307	(200140)			H01L021-00 <--
KR 2001039857	A	20010515	(200167)			H01L029-786
TW 478014	A	20020301	(200305)			H01L021-00 <--
US 6583472	B1	20030624	(200343)			H01L027-01

Application Details

EP 1081676 A1 EP 2000-118783 20000830; JP 2001144301 A JP 2000-253571 20000824; CN 1286493 A CN 2000-126319 20000830; KR 2001039857 A KR 2000-51005 20000831; TW 478014 A TW 2000-116126 20000810; *US 6583472 B1 US 2000-653535 20000831*

Priority Application Information

JP 1999-246798	19990831

Abstract

EP 1081676 A UPAB: 20010421

NOVELTY - A semiconductor device comprises three wirings, three insulating films, a gate electrode and a semiconductor ***film***. The ***second*** wiring and the gate electrode are connected to the first wiring on the ***second*** insulating ***film***. The third wiring is connected to the semiconductor film on the third insulating film.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of manufacturing a semiconductor device comprising forming in sequence (i) the first wiring on a substrate (101) having an insulating surface, (ii) the first insulating film (103) on the first wiring, (iii) the semiconductor film (104) on the first insulating ***film*** , the ***second*** insulating ***film*** (105) on the semiconductor film, (iv) a first contact hole reaching the first wiring, (v) the gate ***electrode*** (106) on the ***second*** insulating ***film overlapping*** a portion of the semiconductor film and connected to the first wiring through the first contact hole, (vi) the third insulating film (108) on the gate ***electrode*** , (vii) a ***second*** contact hole (100a) reaching the semiconductor film, and (viii) the third wiring on the third insulating film connected to the semiconductor ***film*** through the ***second*** contact hole. The first contact hole is formed by selectively etching the first and ***second*** insulating ***films***. The ***second*** contact hole is formed by selectively etching the ***second*** and third insulating ***films***.

USE - As a semiconductor device, e.g. video camera, digital camera, projector, head-mount display, car navigation system, personal computer, information processing terminal or preferably an ***electroluminescent*** (***EL***) display device.

ADVANTAGE - The device does not require a sample hold capacitor in a portion of the peripheral circuit from the fact that the parasitic capacitance of the signal line increases, thus improving the holding characteristics of the

signal line electric potential. The variations in the electric potential of the capacitor wiring caused by a writing-in electric current of a neighboring pixel can be avoided, thus obtaining satisfactory display images.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional structure of an active matrix type liquid crystal display device.

Contact hole 100a
Substrate 101
Scanning line 102
First insulating film 103
Semiconductor film 104
Second insulating ***film*** 105
Gate electrode 106
Third insulating film 108
Dwg.4/19

International Patent Classification

ICM G09G003-36; ***H01L021-00*** ; H01L027-01; H01L029-786
ICS G02F001-1343; G02F001-1345; G02F001-1362; G02F001-1368;
H01L021-3205 ; ***H01L021-768*** ; ***H01L021-822*** ;
H01L027-04; H01L027-12; H01L031-0392; H04N005-66

☐ **L17 ANSWER 21 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-196348 [26] WPIX Full Text

Title

Patterning of organic layers on substrate using inorganic separator stack.

Author/Inventor

PY, C

Patent Assignee/Corporate Source

(CANA) NAT RES COUNCIL CANADA

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
CA 2291302	A1	20010530	(200226)*	EN	24	H01L021-302 <--

Application Details

CA 2291302 A1 CA 1999-2291302 19991130

Priority Application Information

CA 1999-2291302	19991130

Abstract

CA 2291302 A UPAB: 20020424

NOVELTY - Process comprises:

(a) forming a composite stack of at least ***two*** inorganic ***layers*** with different etch rates on a substrate;

(b) masking stack to leave exposed areas defining pattern;

(c) etching away exposed parts to form separators with an ***overhang*** due to different etch rates of inorganic layers; and

(d) depositing an organic layer to form a patterned organic layer between the separators.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) the fabrication of an electronic device using the process above and ***further*** depositing an ***electrode layer*** on the organic layer.

(2) an electronic device produced that comprises at least one patterned layer of organic material and separators.

USE - Used for fabricating electronic components and devices using organic

materials e.g. flat panel displays, semiconductors or conductors for electronic components e.g. transistors, and in passive or active optoelectronic components such as waveguides, modulators and solid state lasers.

ADVANTAGE - The process is simple, gives very high resolution patterns and provides a defect tolerant structure.

DESCRIPTION OF DRAWING(S) - The diagram shows how materials formed on top are discontinuous at the edges of the separators. Dwg.6C/9

International Patent Classification

ICM ***H01L021-302***

ICS G02B006-136; ***H01L021-312***

☐ **L17 ANSWER 22 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2000-553386 [51] WPIX Full Text

Title

CMOS type thin film transistor has channel formation area which overlaps gate insulating film of second TFT which is formed adjacent to first TFT.

Author/Inventor

NAKAJIMA, S

Patent Assignee/Corporate Source

(SEME) SEMICONDUCTOR ENERGY LAB

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
JP 2000216399	A	20000804	(200051)*		28	H01L029-786
US 6420758	**B1**	**20020716**	**(200248)**			**H01L027-01**
US 2002142554	**A1**	**20021003**	**(200267)**			**H01L021-336 <--**

Application Details

JP 2000216399 A JP 1999-327509 19991117; **US 6420758 B1 US 1999-441258 19991116; US 2002142554 A1 Div ex US 1999-441258 19991116,** US 2002-140424 20020506

Priority Application Information

JP 1998-327356	19981117

Abstract

JP2000216399 A UPAB: 20001016

NOVELTY - A channel formation area is formed ***overlapping*** the gate electrode (115) which is formed covering gate electrode (113) of first TFT. A channel formation area is ***overlapped*** with gate insulating ***film*** of ***second*** TFT which is formed adjacent to first TFT. The gate electrode (114) is formed on gate insulating ***film*** of ***second*** TFT. An impurity area is then formed ***overlapping*** the gate insulating film (112).

DETAILED DESCRIPTION - The first TFT has the gate electrode (115) which is formed covering a gate electrode (113) and contacting the gate insulating film (112). An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor device.

USE - For ***electroluminescent*** display device.

ADVANTAGE - Reliability of TFT is increased, by forming N and P type TFT adjacently.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of TFT.

Gate insulating film 112

Gate electrodes 113-115

Dwg.1/24

International Patent Classification

ICM ***H01L021-336*** ; H01L027-01; H01L029-786

ICS G02F001-1365; H01L027-12; H01L031-0392

☐ **L17 ANSWER 23 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2001-267335 [28] WPIX Full Text

Title

Method for providing electroluminescence (EL) display, allocates TFTs with optimum structures to each pixel of EL display based on elements included in pixel.

Author/Inventor

FUKUNAGA, T; YAMAUCHI, Y

Patent Assignee/Corporate Source

(SEME) SEL SEMICONDUCTOR ENERGY LAB; (SEME) SEMICONDUCTOR ENERGY LAB; (SEME) SEMICONDUCTOR ENERGY LAB CO LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 1049176	A2	20001102	(200128)*	EN	30	H01L029-786
JP 2001013893	A	20010119	(200128)		18	G09F009-30
US 6512504	B1	20030128	(200311)			H01L027-01
US 2003132900	A1	20030717	(200348)			G09G003-30
JP 2003317961	A	20031107	(200381)		18	H05B033-14

Application Details

EP 1049176 A2 EP 2000-108848 20000426; JP 2001013893 A JP 2000-124078 20000425; US 6512504 B1 US 2000-551866 *20000418*; US 2003132900 A1 Div ex US 2000-551866 *20000418*, US 2003-337391 20030107; JP 2003317961 A Div ex JP 2000-124078 20000425, JP 2003-27199 20000425

Priority Application Information

JP 1999-119466	19990427

Abstract

EP 1049176 A UPAB: 20010522

NOVELTY - The method forms LDD regions (15)of a switching TFT (201)in a pixel are formed so they do not ***overlap*** gate electrodes (19) to give a structure for reducing an off-current. An LDD region (22) of the current control TFT (202) is formed so it partially ***overlaps*** a gate electrode (35) to give a structure for preventing hot carrier injection and reducing off-current.

DETAILED DESCRIPTION - An independent claim describes an electronic device with at least one pixel.

USE - For providing an ***EL*** display having a high operating performance and reliability.

ADVANTAGE - Provides an active matrix type electronic device with a pixel portion and driving circuit portions provided on the same insulator for providing high operating performance and reliability.

DESCRIPTION OF DRAWING(S) - The drawing shows a sectional structure of a pixel portion of the ***EL*** display.

the LDD regions 15

the switching TFT (201

the gate electrodes 19

further LDD regions 22

a ***further*** gate ***electrode*** 35 Dwg.1/16

International Patent Classification

ICM G09F009-30; G09G003-30; H01L027-01; H01L029-786

ICS ***H01L021-336***

H05B033-14

☐ **L17 ANSWER 24 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1999-357758 [30] WPIX Full Text

Title

Manufacture of an organic thin film device, preferably an emission device.

Author/Inventor

BULOVIC, V; BURROWS, P; FORREST, S R; TIAN, P

Patent Assignee/Corporate Source

(UYPR-N) UNIV PRINCETON

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) WO 9926730	A1	19990603	(199930)*	EN	59	B05D001-32
AU 9916088	A	19990615	(199944)			B05D001-32
US 5953587	**A**	**19990914**	**(199944)**			**H01L051-40**
US 6013538	**A**	**20000111**	**(200010)**			**H01L029-12**
US 6297516	B1	20011002	(200160)			H01L051-10
TW 444235	A	20010701	(200220)			H01L021-00 <--

Application Details

WO 9926730 A1 WO 1998-US25256 19981123; AU 9916088 A AU 1999-16088 19981123; US 5953587 A US 1997-976666 19971124; US 6013538 A US 1997-977205 19971124; US 6297516 B1 Div ex US 1997-976666 19971124, US 1999-344722 19990625; TW 444235 A TW 1998-119394 19981123

Priority Application Information

US 1997-977205	19971124
US 1997-976666	19971124
US 1999-344722	19990625

Abstract

WO 9926730 A UPAB: 19990802

NOVELTY - An organic thin film device is manufactured by depositing organic thin film and electrode layers sequentially through a photolithographic pattern system of insulating layer and photoresist ***overhang***.

DETAILED DESCRIPTION - An organic thin film device is manufactured by: Creating a patterning system comprising an insulation layer and a photoresist layer with a photoresist ***overhang*** on a substrate with contact pads; depositing through the patterning system, in sequence, a first electrode to contact a first contact pad, an organic layer ***overlapping*** the first ***electrode*** and a ***second electrode overlapping*** and contacting the organic ***layer*** and contacting a ***second*** contact pad. The organic layers are preferably organic emission layers. An INDEPENDENT CLAIM is also included for an apparatus for carrying out the above method.

USE - In manufacture of organic ***light emitting devices*** for consumer products, preferably computers, televisions, billboards, signs, vehicles, printers, telecommunications devices, telephones and copiers (claimed).

ADVANTAGE - All the photolithographic steps are completed before the organic films are deposited, the films then being deposited sequentially in a continuous vacuum. This avoids exposure of the organic films to photolithographic solvents.

DESCRIPTION OF DRAWING(S) - The drawing shows a top view of a pattering system as used to deposit a layer from an angle onto a substrate.

Photoresist ***overhang*** 24a

Opening for deposition of material 24b

Layer of material deposited at an angle while the substrate is stationary 25a

Contact pads 21B, 21C and 21D

Dwg.1a/17

International Patent Classification

ICM B05D001-32; ***H01L021-00*** ; H01L029-12; H01L051-10; H01L051-40
ICS H01L033-00

☐ **L17 ANSWER 29 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1991-067363 [10] WPIX Full Text

Title

Mfg. flat LCD with inverted structure - using multilayer structure deposited on glass substrate and photoetched while polyamide covers lines formed and exposing to UV light.

Author/Inventor

CHOUAN, Y; VINOUZE, B

Patent Assignee/Corporate Source

(ETFR) FRANCE TELECOM; (ETFR) ETAT FRANCAIS; (ETFR) FRENCH GOVERNMENT

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 415842	A	19910306	(199110)*			
FR 2651371	A	19910301	(199119)			
US 5015597	**A**	**19910514**	**(199122)**			

Application Details

EP 415842 A EP 1990-402376 19900828; US 5015597 A US 1990-573340 19900824; JP 03119320 A JP 1990-227869 19900829; EP 415842 B1 EP 1990-402376 19900828; DE 69008082 E DE 1990-608082 19900828, EP 1990-402376 19900828

Priority Application Information

FR 1989-11331	19890829

Abstract

EP 415842 A UPAB: 19941216

The display includes a glass substrate (10) on which a structure of metallic, insulating, semiconducting and metallic layers (12, 14, 16, 18, 20) is formed. The insulating and semiconducting layers are deposited by PECVD in a single cycle. The multilayer structure is subsequently etched so that parallel lines are obtained on the substrate.

The lines are covered by a negative photosensitive polyamide (22) that is exposed to UV light through the glass substrate. The lines on the substrate act as optical masks. The masked regions of the polyamide aree then eliminated and the remaining polyamide is quenched. A conducting transparent layer (30) is then deposited on top. This layer is photoetched so that screen pixels are defined.

USE/ADVANTAGE - For manufacturing ***electroluminescent*** , electrochromic or electrolytic displays. Is simple, reliable and ensures improved contact between transistor source and drain. Semiconducting layer thickness is not critical and eliminates use of non-flat surfaces. @(11pp Dwg.No.9/10)@

9/10

Abstract, Equivalent

EP 415842 B UPAB: 19940531 Process for producing a wall for an active matrix display screen, characterized in that it comprises depositing on a transparent substrate (10) a stack of layers constituted by a first metallic layer (12), an insulating layer (14), a semiconductor layer (16), a highly doped semiconducting ***layer*** (18) and a ***second*** conducting ***layer*** (20), a first photoetching takes place through a first masking level so as to only leave behind the stack lines (L1, L2, L3, etc), the substrate and lines are covered with negative photosensitive material (22) in order to obtain, between the stack lines, a layer having a thickness equal to that of said stack, the assembly is irradiated

through the transparent substrate (10), the first metallic layer (12) of the stack rows serving as an opaque mask, the non-irradiated resin located above the stack rows is removed, said resin only being left between the stack rows (L1, L2, etc.), followed by the planarisation of the assembly and the annealing of the resin, a transparent conductive layer (30) is deposited on the assembly and said layer undergoes photo-etching to form a second masking level, defining columns and blocks provided with a finger parallel to the columns, the columns and block fingers ***overlapping*** the stack rows (L1, L2, L3, etc.) and the columns and blocks, as well as the fingers of the latter are used as a mask for etching the ***second*** conductive ***layer*** (20) and the doped semiconducting (18), which leaves transistors (T) having as the gate (G) the first metallic layer (12) deposited on the substrate, as the drain (D) and block finger, as the source (S) the column and as the channel (Ch) the semiconducting layer (16) beneath the etched zone between the column and the block finger. Dwg.1/10

International Patent Classification

G02F001-13; G03C005-00; G09F009-35; ***H01L021-84*** ; H01L027-12; H01L029-78
ICM G02F001-136
ICS G02F001-13; G03C005-00; G09F009-35; ***H01L021-84*** ; H01L027-12; H01L029-78; H01L029-784
ICS G02F001-13; G03C005-00; G09F009-35; ***H01L021-84*** ; H01L027-12; H01L029-78; H01L029-784

☐ **L17 ANSWER 30 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1986-313195 [48] WPIX Full Text

Title

Electrode system for semiconductor device especially CCD - comprises series electrode strips on insulating layer separated by grooves containing conductor material constituting second electrodes.

Author/Inventor

DAVIDS, G J

Patent Assignee/Corporate Source

(PHIG) PHILIPS GLOEILAMPENFAB NV

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 4754311	**A**	**19880628**	**(198828)**			
US 4766089	**A**	**19880823**	**(198836)**			

Priority Application Information

NL 1985-1339	19850510

Abstract

EP 202704 A UPAB: 19930922

Parallel, coplanar, interleaved arrays of ***electrodes*** (1, ***2***) supply a device via metal tracks (10A,10B) connected to a clock voltage source. The electrodes (1) of the first set are contacted through windows (7) formed in an insulating overlayer, which ***overlap*** the adjacent ***second electrodes*** (***2***). The ***electrodes*** of the ***second*** set are contacted through windows (8) in a thinner, insulating overlayer, and exhibit breaks (9) between the windows (8) and the ***overlapping*** first contact windows (7), and also between the first conductor windows. Both first and ***second electrodes*** are of silicon, with the insulating material outside the contact windows comprised of silicon nitride and silicon oxide layers.

ADVANTAGE - Permits increased packing density, facilitates manufacture, and avoids shorting between adjacent conductors. 1/10

International Patent Classification

H01L021-28 ; H01L027-10; H01L029-60

☐ **L17 ANSWER 32 OF 33 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1977-57479Y [32] WPIX Full Text

Title

Thin film transistor containing indium in semiconductor layer - pref. of cadmium selenide to increase stability and transconductance.

Patent Assignee/Corporate Source

(WESE) WESTINGHOUSE ELECTRIC CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 4040073	**A**	**19770802**	**(197732)***			
DE 2704312	A	19780223	(197809)			
JP 53026586	A	19780311	(197816)			
GB 1565551	A	19800423	(198017)			
JP 61026233	B	19860619	(198629)			

Priority Application Information

US 1976-716046	19760820

Abstract

US 4040073 A UPAB: 19930901

A thin film transistor formed on an insulating substrate has a semiconductive layer, pref. CdSe, having sufficient In incorporated in the layer to stabilise the device. The source and drain contracts comprise an In layer covered by a Cu layer.

The transistor comprises (a) a first conductive gate on the substrate, (b) an insulating layer on the gate, with the gate extending beyond the layer, (c) a semiconductor layer on the insulator and overlying (pt. of) the gate, (d) source and drain contacts ***overlapping*** opposed sides of the semiconductor ***layer*** , (e) a ***second*** insulating ***layer*** on the semiconductor and pt. of source and drain contacts and (f) a second conductive gate on the second insulator. The second gate is electrically connectable to the first gate.

The transistor is useful for display devices, e.g. liquid crystals or ***electroluminescent phosphor*** devices. The incorporated In reduces charge trapping, increasing stability especially at high frequencies, and increases trans-conductance. The contacts enable devices to be made that can withstand >350V without breakdown or collapse.

International Patent Classification

H01L021-36 ; H01L027-12; H01L029-22; H01L049-02